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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant: Dennis M. O'Connor	§	Art Unit:	2188
Serial No.: 09/928,671	§	Examiner:	Pierre M. Vital
Filed: August 13, 2001	§		
For: Cache Architecture to Reduce Leakage Power Consumption	§	Atty Docket:	ITL.0606US P11747

Mail Stop **Appeal Brief-Patents**
Commissioner for Patents
P.O. Box 1450
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APPEAL BRIEF

Date of Deposit: October 7, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Cynthia L. Hayden

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-6, 8-16, 18-26, and 28-30 are rejected. Each rejection is appealed.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

Claim 1 calls for a multilevel cache having a core having relatively faster components and a region including relatively slower components. Relatively slower devices may be provided by an L2 cache implemented with slower devices. See page 4, lines 3-9 of the specification and Figure 1. See, also, page 5, lines 1-5. According to the claim, the line replacement policy is implemented by the region including slower components which, in this example, would be the L2 cache. See page 6, line 24 through page 7, line 4.

Claim 11 corresponds as an article claim to method claim 1. Claim 21 corresponds as a system claim to method claim 1.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Are Claims 1-2, 5, 8, 11, 12, 15, 18, 21-22, 25, and 28 Anticipated by Arimilli?

ARGUMENT

A. **Are Claims 1-2, 5, 8, 11, 12, 15, 18, 21-22, 25, and 28 Anticipated by Arimilli?**

Claim 1 calls for defining a multilevel cache including a core having relatively faster components and a region including relatively slower components. The line replacement policy is implemented in the region including relatively slower components.

The Examiner contends that Arimilli discloses a core having relatively faster components because the L1 cache is faster since it is closer to the processor core. But the argument fails on its face. Just because the core is closer to the L1 cache does not mean that the L1 cache has faster components, it just means that because the L1 cache is closer to the core it can get its results to the core faster than the L2 cache can get its results to the core.

Thus, the argument that "L1 cache is faster since it is closer to processor core" is not strictly speaking correct. The core is no faster because of where it is located. It just gets its results to the processor faster, according to the Examiner. The language of claim 1 is that the cache has a core having relatively faster components and a region including relatively slower components. (In the claim, the core is part of the cache, while in the office action a processor core, which is presumably part of the processor itself, is referred to).

Also, in paragraph 6 of the office action, it is indicated that column 2, lines 34-46, shows that there are different speed components in the L1 and L2 caches. However, nothing in any of that material supports the assertions based on that material. In other words, there is nothing therein suggesting using faster components in one of the L1 and L2 caches.

To clarify, all of the components of the L1 and the L2 cache may have exactly the same speeds in Arimilli and still the processor can execute the instructions from the L1 cache faster from the time they are sent because the L1 cache is closer to the processor so the processor returns the results more quickly. However, this location does not give any reason to believe that, inherently, the components of the L1 or the L2 cache are of different speeds. Therefore, there is no basis for the Section 102 rejection and it should be reversed.

Respectfully submitted,

Date: October 7, 2004

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CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:

defining a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

implementing a line replacement policy in said region.

2. The method of claim 1 including managing the core from a level 2 cache.

3. The method of claim 1 including using a virtual address to index the core to avoid the need for an address translation mechanism.

4. The method of claim 1 including placing functions relating to tags and valid bits as well as the data itself in the core.

5. The method of claim 1 including using a write-through core cache.

6. The method of claim 1 including performing virtual-to-physical translation in said region.

8. The method of claim 1 including handling a core cache miss by passing details of an access to said region.

9. The method of claim 8 including enabling said region to use a memory translation mechanism to determine the physical address and attributes of the access.

10. The method of claim 9 including checking to see if requested data is in a storage associated with said region.

11. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

define a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

implement a line replacement policy in said region.

12. The article of claim 11 further storing instructions that enable the processor-based system to manage the core from a level 2 cache.

13. The article of claim 11 further storing instructions that enable the processor-based system to use a virtual address to index the core to avoid the need for an address translation mechanism.

14. The article of claim 11 further storing instructions that enable the processor-based system to access functions relating to tags and valid bits as well as the data itself in the core.

15. The article of claim 11 further storing instructions that enable the processor-based system to use a write-through core cache.

16. The article of claim 11 further storing instructions that enable the processor-based system to perform virtual-to-physical translation in said region.

18. The article of claim 11 further storing instructions that enable the processor-based system to handle a core cache miss by passing details of an access to said region.

19. The article of claim 18 further storing instructions that enable the processor-based system to enable said region to use a memory translation mechanism to determine the physical address and attributes of the access.

20. The article of claim 19 further storing instructions that enable the processor-based system to check to see if requested data is in a storage associated with said region.

21. A system comprising:

a processor;

a multilevel cache including a core having relatively faster components and a region including relatively slower components; and

said region to implement a line replacement policy.

22. The system of claim 21 wherein said core is a level 1 cache and said region is a level 2 cache.

23. The system of claim 21 wherein said storage stores instructions that enable the processor to use a virtual address to index the core to avoid the need for an address translation mechanism.

24. The system of claim 21 wherein said storage stores instructions that enable the processor to place functions relating to tags and valid bits as well as the data itself in the core.

25. The system of claim 21 wherein said core cache is a write-through cache.

26. The system of claim 21 wherein said storage stores instructions that enable the processor to perform virtual-to-physical translation.

28. The system of claim 21 wherein said storage stores instructions that enable the processor to handle a core cache miss by passing details of an access to said region.

29. The system of claim 28 wherein said storage stores instructions that enable the processor to enable said region to use a memory translation mechanism to determine the physical address and attributes of the access.

30. The system of claim 29 wherein said storage stores instructions that enable the processor to check to see if requested data is in a storage associated with said region.

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. ITL.0606US

In Re Application Of: **Dennis M. O'Connor**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/928,671	August 13, 2001	Pierre M. Vital	21906	2188	8164

Invention: **Cache Architecture to Reduce Leakage Power Consumption**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **September 14, 2004.**

The fee for filing this Appeal Brief is: **$340.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

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Signature

Dated: **October 7, 2004**

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